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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/034,219	12/28/2001	Toni Juan	1662-47000 (P01-3694)	9074

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EXAMINER
O BRIEN, BARRY J

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,219	JUAN ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/28/01, 4/01/02, 5/14/02, and 6/30/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/01/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: IDS as received on 4/01/02, Extension of Time as received on 5/14/02, Declaration and Fee as received on 5/14/02, Change of Address as received on 6/30/03, and Formal Drawings as received on 6/30/03.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

Claim Objections

5. Claim 14 is objected to because of the following informalities:

   a. Claim 14 recites the limitation, "The method of claim 13" on its first line. There is a lack of antecedent basis in the claims for this limitation. Please correct the

claim language to read, "The system of claim 13" to provide the correct antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Merchant et al., U.S. Patent No. 6,665,792.

8. Regarding claims 1, 10 and 19, taking claim 10 as exemplary, Merchant has taught a computer system, comprising:

a. A microprocessor (100 of Fig.1),

b. An input device coupled to said microprocessor (IQ, 112 of Fig.1),

c. Memory coupled to said microprocessor, said memory containing executable instructions (104 of Fig.1),

d. Wherein said microprocessor:

I. Fetches instructions from said memory (see Col.3 line 54 – Col.4 line 8), certain fetched instructions being load instructions (loads) and causing

load operations, and other fetched instructions being store instructions (stores) and causing store operations (see Col.1 line 56 – Col.2 line 2),

II. Executes the fetched instructions out of program order (see Col.6 lines 4-16),

III. Detects a load/store order violation wherein a load executes prior to a store on whose data the load depends (see Col.7 lines 28-45 and Col.8 line 41 - Col.9 line 30),

IV. Creates a store set for the load (see Col.3 lines 25-40, Col.11 lines 1-41 and Col.12 lines 3-22, 26-43),

V. Adds the store to the store set (see Col.3 lines 25-40, Col.11 lines 1-41 and Col.12 lines 3-22, 26-43). Here, a "store set" corresponding to entries in the load buffer, the store buffer and the bus queue is created upon detecting of a load/store order violation by making entries for the corresponding load and store instructions in their respective buffers (see Col.3 lines 25-40), as well as setting the invalid store flag in the store buffer (see Col.11 lines 1-41) and the inhibit load flag in the bus queue (see Col.12 lines 3-22), with the entries in the buffers being indexed by the sequence number and source/destination addresses of the instructions (see Col.12 lines 26-43).

VI. Determines whether the store is poisoned by a previously poisoned instruction (see Col.11 lines 13-41). Here, it is determined if there have been more than one store instructions with invalid (poison) flags, which

causes the prior load instructions to be replied (see Col.11 lines 26-31). Thus, the current store instruction has been poisoned (invalidated) by a previously poisoned (invalidated) instruction.

VII. If the store is poisoned, sets a poison value that indicates that the store is poisoned (see Col.11 lines 13-41). Here, the store invalid flag (510 of Fig.5) acts as a poison value (see Col.10 lines 54-59 and Col.11 lines 22-41).

VIII. Re-processes said load if said poison value associated with said store indicates the store has been poisoned (see Col.11 lines 13-41).

9. Claims 1 and 19 are nearly identical to claim 10. Claim 1 lacks the hardware structure of claim 10, and claim 19 lacks the input device of claim 10. However, both claims 1 and 19 encompass the same scope as claim 10. Therefore, claims 1 and 19 are rejected for the same reasons as claim 10.

10. Regarding claims 2, 11 and 20, taking claim 11 as exemplary, Merchant has taught the system of claim 10, wherein said poison value comprises a bit in a table (see Col.10 lines 54-59 and Col.11 lines 22-41).

11. Claims 2 and 20 are nearly identical to claim 11, differing in their parent claims, but encompassing the same scope as claim 11. Therefore, claims 2 and 20 are rejected for the same reasons as claim 11.

12. Regarding claims 3, 12 and 21, taking claim 12 as exemplary, Merchant has taught the system of claim 10, wherein the store set includes a pointer that points to the poison value (see Col.12 lines 26-43). Here, since there is a pointer to a store instruction (destination address) that

is contained in the store set tables, and the poison value is directly associated with the store instruction (see Fig.5 and Col.10 lines 54-59), there is a pointer to the poison value associated with that store instruction.

13. Claims 3 and 21 are nearly identical to claim 12, differing in their parent claims, but encompassing the same scope as claim 12. Therefore, claims 3 and 21 are rejected for the same reasons as claim 12.

14. Regarding claims 4, 13 and 22, taking claim 13 as exemplary, Merchant has taught the system of claim 10, wherein said store set includes a pair of tables which are used to identify said store instruction (see Col.11 lines 22-41 and Col.12 lines 26-43). Here, entries in the load buffer, the memory ordering buffer, and the load buffer are all used in identifying a invalid store instruction.

15. Claims 4 and 22 are nearly identical to claim 13, differing in their parent claims, but encompassing the same scope as claim 13. Therefore, claims 4 and 22 are rejected for the same reasons as claim 13.

16. Regarding claims 5, 14 and 23, taking claim 14 as exemplary, Merchant has taught the system of claim 13, wherein said microprocessor clears said poison value when said store is no longer poisoned (see Col.3 lines 28-39).

17. Claims 5 and 23 are nearly identical to claim 14, differing in their parent claims, but encompassing the same scope as claim 14. Therefore, claims 5 and 23 are rejected for the same reasons as claim 14.

18. Regarding claims 6, 15 and 24, taking claim 15 as exemplary, Merchant has taught a computer system, comprising:

a. A microprocessor (100 of Fig.1),

b. memory coupled to said microprocessor (104 of Fig.1), said memory containing a store instruction (store) and a load instruction (load) that target a common memory location (see Col.1 line 56 – Col.2 line 2),

c. Wherein said microprocessor:

I. Fetches said load and store (see Col.3 line 54 – Col.4 line 8),

II. Determines if the data to be written by said store is stale (see Col.7 lines 28-45 and Col.8 line 41 - Col.9 line 30),

III. If said data is stale, sets a value associated with said store (see Col.11 lines 13-41). Here, the store invalid flag (510 of Fig.5) acts as a poison value (see Col.10 lines 54-59 and Col.11 lines 22-41),

IV. If said value is set, re-processes said load to execute after said data is no longer stale (see Col.11 lines 13-41).

19. Claims 6 and 24 are nearly identical to claim 15. Claim 6 lacks the hardware structure of claim 15, and claim 24 lacks the system of claim 15. However, both claims 6 and 24 encompass the same scope as claim 15. Therefore, claims 6 and 24 are rejected for the same reasons as claim 15.

20. Regarding claims 7, 16 and 25, taking claim 16 as exemplary, Merchant has taught the system of claim 15, wherein said microprocessor establishes a store set for said load to include said store (see Col.3 lines 25-40, Col.11 lines 1-41 and Col.12 lines 3-22, 26-43). Here, a "store set" corresponding to entries in the load buffer, the store buffer and the bus queue is created upon detecting of a load/store order violation by making entries for the corresponding load and store

instructions in their respective buffers (see Col.3 lines 25-40), as well as setting the invalid store flag in the store buffer (see Col.11 lines 1-41) and the inhibit load flag in the bus queue (see Col.12 lines 3-22), with the entries in the buffers being indexed by the sequence number and source/destination addresses of the instructions (see Col.12 lines 26-43).

21. Claims 7 and 25 are nearly identical to claim 16, differing in their parent claims, but encompassing the same scope as claim 16. Therefore, claims 7 and 25 are rejected for the same reasons as claim 16.

22. Regarding claims 8, 17 and 26, taking claim 17 as exemplary, Merchant has taught the system of claim 16, wherein said microprocessor uses said store set to access said value (see Col.12 line 62 – Col.13 line 10). Here, the processor has to access the memory order buffer and store buffer and the load buffer, which are the tables used in the store set, in order to check for an entry in the store buffer that is both older than a load instruction and has its invalid (poison) flag set.

23. Claims 8 and 26 are nearly identical to claim 17, differing in their parent claims, but encompassing the same scope as claim 17. Therefore, claims 8 and 26 are rejected for the same reasons as claim 17.

24. Regarding claims 9, 18 and 27, taking claim 18 as exemplary, Merchant has taught the system of claim 15, wherein said value comprises a poison bit (see Col.10 lines 54-59 and Col.11 lines 22-41).

25. Claims 9 and 27 are nearly identical to claim 18, differing in their parent claims, but encompassing the same scope as claim 18. Therefore, claims 9 and 27 are rejected for the same reasons as claim 18.

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

27. Akkary, U.S. Patent No. 6,463,522 has taught a processor which uses a load and store buffer in order to maintain data coherency between dependent threads.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

29. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien

Examiner
Art Unit 2183

BJO
7/12/2004

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